Notice of Allowability	Application No.	Applicant(s)	
	10/811,618	TELESCO, WILLIAM JAMES	
	Examiner	Art Unit	
	Ernest Unelus	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/28/06*.

2. ☒ The allowed claim(s) is/are *62-66 and 68-70*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

I. EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Mr. Eric J. Baron (Reg. No. 56,025) on March 02, 2007. The examiner proposed amendments to better place the application in condition for allowance, particularly adding the limitation that prior arts fail to teach. Mr. Baron agreed.

3. The application has been amended as follows:

5. **Claim 62.** (CURRENTLY AMENDED) In a computer, having a plurality of computer resources including a processor and memory, a controller and resource management system, wherein said controller and resource management system is implemented in electronic hardware that is physically separate and functionally independent of said processor, said controller and resource management system comprising:

a watchdog timer function for monitoring the health and operation of said controller and resource management system;

a configuration and device driver function for configuring said plurality of computer resources;

a plurality of computer input/output interfaces for coupling said controller and resource management system to said plurality of computer resources, including a computer input/output interface for communicatively coupling control messages to said processor;

a plurality of buffers for buffering data coupled to said plurality of computer input/output interfaces, including an application program interface (API) buffer for communicatively coupling control messages to said processor;

a memory controller for controlling memory data communications between said memory and said controller and resource management system;

an input/output controller for coupling said controller and resource management system to said plurality of computer input/output interfaces; [[.]]

event priority and scheduler logic which inputs said memory data via said memory controller, and inputs computer events via said input/output controller, and responsive to said inputs, outputs data comprising: prioritized and scheduled computer events, prioritized and scheduled computer memory data; and

security filter logic which inputs said prioritized and scheduled data, and responsive to said inputs, outputs data comprising: filtered and verified computer events, filtered and verified computer memory data, and responsive to said output, communicatively couples said output to said processor such that prioritized, and scheduled, and verified computer events and computer memory data is coupled to said processor through said controller and resource management system; and, wherein said controller and resource management system does not require processor executable instructions to operate.

6. **Claim 69.** (CURRENTLY AMENDED) In a personal computer, having a plurality of personal computer resources including a processor and memory, a controller and resource management system, wherein said controller and resource management system is implemented in

electronic hardware that is physically separate and functionally independent of said processor, said controller and resource management system comprising:

a watchdog timer function for monitoring the health and operation of said controller and resource management system;

a configuration and device driver function for configuring said plurality of personal computer resources;

a plurality of personal computer input/output interfaces for coupling said controller and resource management system to said plurality of personal computer resources, including a personal computer input/output interface for communicatively coupling control messages to said processor;

a plurality of buffers for buffering data coupled to said plurality of personal computer input/output interfaces, including an application program interface (API) buffer for communicatively coupling control messages to said processor;

a memory controller for controlling memory data communications between said memory and said controller and resource management system;

an input/output controller for coupling said controller and resource management system to said plurality of personal computer input/output interfaces; [[.]]

event priority and scheduler logic which inputs said memory data via said memory controller, and inputs personal computer events via said input/output controller, and responsive to said inputs, outputs data comprising: prioritized and scheduled personal computer events, prioritized and scheduled personal computer memory data; and

security filter logic which inputs said prioritized and scheduled data, and responsive to said inputs, outputs data comprising: filtered and verified personal computer events, filtered and verified personal computer memory data, and responsive to said output, communicatively couples said output to said processor such that prioritized, and scheduled, and verified personal computer events and personal computer memory data is coupled to said processor through said controller and resource management system; and, wherein said controller and resource management system does not require processor executable instructions to operate.

Claims 70. (CURRENTLY AMENDED) A method for controlling and managing a plurality of computer resources, including a processor for performing a plurality of processes, and handling a plurality of computer events and memory data such that said method is functionally independent of said processor, said method comprising:

controlling and receiving said memory data communications via a memory controller;

controlling input/output interfaces via an input/output controller;

receiving said plurality of computer events via said input/output controller;

providing a security function for filtering and verifying said plurality of computer events and said memory data, and further notifying said plurality of computer resources of said plurality of computer events and said memory data such that said security function is functionally independent of said processor, and such that said plurality of computer events and said memory data are filtered and verified prior to arrival at said processor;

managing and scheduling said plurality of processes performed by said processor;

prioritizing said plurality of processes performed by said processor;

configuring a watchdog timer and reacting to a timeout event of said watchdog timer ; and

configuring said plurality of computer resources via a configuration and device driver function.

Claims 67 and 71 – 74 have been canceled by the applicant.

II. RELEVANT ART CITED BY THE EXAMINER

1. The following prior art made of record and not relied upon is cited to establish the level of skill in the applicant's art and those arts considered reasonably pertinent to applicant's disclosure. See **MPEP 707.05(c)**.

2. The following references teaches a computer, having a plurality of computer resources including a processor and memory, a controller and resource management system to provide security.

U.S. PATENT NUMBER

US pub. 2005/0114687

US pub. 2005/0071668

US pub. 2004/0215992

US pub. 2003/0237007

US pat. 7,024,695

III. REASONS FOR ALLOWANCE

1. **claims 62-66 and 68-70** are allowed.

2. The following is an examiner's statement of reasons for allowance:

The primary reasons for allowance of claims 62-66 and 68-70 in the instant application is the combination with the inclusion in these claims that the **event priority and scheduler logic which inputs said memory data via said memory controller, and inputs computer events via said input/output controller, and responsive to said inputs, outputs data comprising: prioritized and scheduled computer events, prioritized and scheduled computer memory data; and security filter logic which inputs said prioritized and scheduled data, and responsive to said inputs, outputs data comprising: filtered and verified computer events, filtered and verified computer memory data, and responsive to said output, communicatively couples said output to said processor such that prioritized, and scheduled, and verified computer events and computer memory data is coupled to said processor through said controller and resource management system; and, wherein said controller and resource management system does not require processor executable instructions to operate**. The prior art of record neither anticipates nor renders obvious the above recited combination.

3. Per the instant office action, **claims 62-66, 69, and 70 (Now renumbered to claims 1-8)** are considered as allowable subject matter.

4. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

DIRECTION OF FUTURE CORRESPONDENCES

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ernest Unelus whose telephone number is (571) 272-8596. The examiner can normally be reached on Monday to Friday 9:00 AM to 5:00 PM.

IMPORTANT NOTE

6. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Donald Sparks, can be reached at the following telephone number: Area Code (571) 272-4201.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PMR system, see her//pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217- 91 97 (toll-free).

March 02, 2007

Ernest Unelus
Patent Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

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March 02, 2007

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